Remarks

In the instant Office Action, the Examiner stated: "The Non-Patent Literature cited in the IDS filed on 12/15/2004, is not currently part of the electronic file. Consequently, the NPL for IDS has not been considered." Applicant respectfully requests the Examiner to consider the submitted NPL which should now be part of the electronic file.

In the Office Action, the Examiner noted that claims 31-38, 43-68, and 70 are pending in the application, and that claims 31-38, 43-68, and 70 are rejected. By this amendment, claims 32-33, 66-68, and 70 have been canceled, and claims 31, 34, 37-38, and 43-50 have been amended. Thus, claims 31, 34-38, and 43-65 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Claims

Rejection Under 35 USC 112, second paragraph

The Examiner rejected claims 31, 32, and 43-49 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention as having insufficient antecedent basis. Applicant has amended the claims to supply the required antecedent basis.

Rejection Under 35 USC 102(b)

The Examiner rejected claims 31-33 under 35 U.S.C. § 102(b) as being anticipated by *Black et al.*, U.S. Patent No. 5,761,723 (hereinafter *Black*). Applicant respectfully traverses.

With respect to claim 31, which as amended includes the limitations of now canceled claim 32, the Examiner states in the Office Action with respect to claim 32 that each instruction of *Black* would have a HIT?MISS indicator. However, amended claim 31 specifically recites an indicator is associated with each byte of each variable byte-length instruction stored in the instruction buffer and each indicator indicates whether the byte is predicted by the BTAC as an opcode byte of one of the previously executed branch instructions, which *Black* does not teach. It is not surprising that *Black* does not store

such an indicator for each byte of each instruction because *Black* teaches a microprocessor with the PowerPC architecture, which has fixed-length instructions (see col. 6, line 67; col. 7, line 65; col. 9, line 11; col. 10, line 62; col. 11, line 26); hence, the location of the opcode byte of the fixed length instructions within *Black*'s instruction buffer would be known. In contrast, amended claim 31 recites a variable byte-length instruction processor. Applicant respectfully asserts that *Black* does not anticipate claim 31 and respectfully requests the Examiner withdraw the rejection.

Rejection Under 35 USC 103

The Examiner rejected claims 34-36, 50-55, and 59-65 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell et al.*, U.S. Patent No. 5,850,543 (hereinafter *Shiell*) in view of *Hsu et al.*, U.S. Patent No. 5,948,100 (hereinafter *Hsu*). Applicant respectfully traverses.

With respect to amended claims 34 and 50, Applicant asserts that *Hsu* has not taught a bit associated with each branch instruction which is true only if the associated branch instruction spans more than one instruction cache line, as recited in amended claims 34 and 50. Therefore, Applicant respectfully requests the Examiner withdraw the rejections.

Applicant respectfully asserts *Shiell* in view of *Hsu* does not obviate dependent claims 35-38 and 51-65 because they depend from amended independent claims 34 and 50, respectively, which are not obviated by *Shiell* in view of *Hsu* for the reasons discussed above.

The Examiner rejected claims 37-38 under 35 U.S.C. § 103(a) as being unpatentable over *Shiell* in view of *Hsu* and further in view of *Black*. Applicant respectfully traverses.

Applicant respectfully asserts that *Shiell* in view of *Hsu* and further in view of *Black* does not obviate amended claims 37 and 38 for the reasons discussed above with respect to claim 31.

The Examiner rejected claims 43-44 and 46-49 under 35 U.S.C. § 103(a) as being unpatentable over *Black* and taking Official Notice of and/or finding inherent various claim limitations. Applicant respectfully traverses.

Applicant respectfully asserts *Black* does not anticipate or obviate dependent claims 43-49 because they depend from amended independent claim 31, which is not anticipated or obviated by *Black* for the reasons discussed above.

Further with respect to amended claim 43, the Examiner stated that variable byte-length instruction processors exist, and also stated: "Consequently, in order to make *Black*'s system capable of executing variable length instructions ...". The Examiner appears to be assuming that it would be a simple matter to make *Black*'s processor capable of predicting branch instructions among variable length instructions, buffering the variable length target instructions, and properly checking the prediction within a variable length instruction stream. Applicant respectfully disagrees, and asserts that *Black*'s processor is relatively simple with respect to branch prediction, instruction buffering, and branch prediction checking due to its fixed length instructions. Applicant asserts that making *Black*'s processor capable of processing variable byte-length instructions with respect to branch prediction, instruction buffering, and branch prediction checking would have been complex at the time Applicant's invention was made without the benefit of Applicant's present disclosure as a roadmap for reconstructing Applicant's invention; therefore, Applicant's invention would have been non-obvious to a person of ordinary skill in the art at the time the invention was made. Consequently, Applicant respectfully asserts the rejection is improper.

With respect to amended claim 48, the Examiner equates a resolved target address with a non-speculative branch target address prediction, which is recited in claim 48. Applicant respectfully asserts that a resolved target address is not a non-speculative branch target address prediction as recited in claim 48, for reasons similar to those provided in Applicant's November 29, 2004 response to the Examiner's August 31, 2004 Office Action.[1] A non-speculative prediction is non-speculative because it is at least known at

[1] The relevant text of Applicant's previous response is: "Paragraphs 96-103 of Applicant's specification describe in great detail the distinction between speculative and non-speculative predictions as the Applicant has defined them. In particular, paragraph 101 teaches that a non-speculative prediction is a prediction made with the certainty that a branch instruction exists in the current instruction stream because the branch instruction has been decoded by instruction decode logic; nevertheless, the non-speculative prediction is still a prediction because, for example, if the branch instruction is a conditional branch instruction, the branch may or may not be taken in any given execution of the branch instruction. This is in contrast to a speculative prediction, which is made without certainty that a branch instruction resides in the cache line

the time the non-speculative prediction is made that a branch instruction is present in the cache line selected by the fetch address due to decoding of the instruction (in contrast to a speculative prediction for which it is not known at the time the speculative prediction is made that a branch instruction is present in the cache line selected by the fetch address); nevertheless, the non-speculative prediction – unlike a resolved target address – is still a prediction because it may be wrong, as determined later when compared to the resolved target address, for example, in the cases of an x86 indirect jump through memory and self-modifying code, as discussed in paragraphs 102 and 103 of Applicant's specification. For this reason, Applicant respectfully asserts *Black* does not obviate claim 48, and respectfully requests the Examiner withdraw the rejection.

Applicant respectfully asserts *Black* does not obviate claim 49 for reasons similar to those stated above with respect to claim 48, and respectfully requests the Examiner withdraw the rejection.

The Examiner rejected claim 45 under 35 U.S.C. § 103(a) as being unpatentable over *Black* in view of *Stiles*, U.S. Patent No. 5,513, 330, and further in view of *Sinharoy*, U.S. Patent No. 6,457,120. Applicant respectfully traverses.

Applicant has amended claim 45 to clarify that it is the length of previously executed branch instructions which is cached in the BTAC and subsequently compared with the instruction length determined by the instruction decode logic. Applicant respectfully asserts that *Stiles* does not teach this limitation. Therefore, Applicant respectfully asserts *Black* in view of *Stiles* and further in view of *Sinharoy* does not obviate amended claim 45, and respectfully requests the Examiner withdraw the rejection.

For all of the reasons advanced above, Applicant respectfully submits that claims 31, 34-38, and 43-65 are in condition for allowance. Reconsideration of the rejections is requested, and Allowance of the claims is solicited.

---

selected by the instruction cache fetch address, which is used by the BTAC to predict the branch instruction. See paragraph 96. ... [T]he claims are read in light of the specification, and Applicant may be his own lexicographer."

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

Respectfully submitted,

E. Alan Davis

E. Alan Davis
Huffman Law Group, P.C.
Registration No. 39,954
Customer No. 23669
1832 N. Cascade Ave.
Colorado Springs, CO 80907
512.301.7234
719.623.0141 fax
alan@huffmanlaw.net

Date: 4-23-05

"EXPRESS MAIL" mailing label number EO 004 581 310 VS. Date of Deposit 4/25/05. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA, 22313.

By: